AMENDMENTS TO THE SPECIFICATION

At page 9 please replace the paragraph commencing at line 19 with the following amended paragraph:

The filter 700 is a low-pass filter and includes a first and second resistor R1, R2, a first and second capacitor C1, C2, and a first and second switches SW1, SW2. The first capacitor C1 is connected between a positive input node and a positive output node. The second capacitor C2 is connected between a negative input node and a negative output node. The first resistor R1 and the first switch SW1 are serially connected between the positive output node and a bias voltage VBIAS node. The second resistor R2 and the second switch SW2 are serially connected between the negative output node and the bias voltage VBIAS node.

At page 10 please replace the paragraph commencing at line 19 with the following amended paragraph:

In FIG. 14, if a resistor with low resistance is used, instead of the resistor R1 and the switch SW1, and the input signal VIN is transferred to the gate of ~~the~~ a MOS transistor ~~M2~~ M1, a large amount of signal loss occurs in the input signal VIN. This is because the input signal VIN is transferred to the bias circuit 810. In order to reduce loss in the input signal VIN, the bias circuit 810 should have a high resistance. However, a high resistance results in high parasitic capacitance and a large chip size. These problems can be solved by connecting the resistor R1 to the switch and scaling the resistance to a large value. In addition, frequency characteristics can be controlled by scaling the resistance, thereby allowing transmission of an input signal at a low frequency.